TEXAS INSTRUMENTS

Designer's Reference Guide

Logic and Linear Sections

Supplement

1988   *Military Products*

Supplement to 1988 Edition Military Products Designer's Reference Guide

Logic and Linear Sections

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

MILITARY PRODUCT FLOWS

Process Level	Prefix Suffix	Description
JM38510 Class B	JM38510	Qualified per MIL-M-38510 Class B. Produced in DESC certified production facilities.
DESC	SNJ,B	Certified and symbolized to the DESC Military Drawing where TI is an approved source.
Class B	SNJ	Screened per requirements of MIL-STD-883 Class B Method 5004. Conforms to the requirements of JEDEC Publication 101.
Military Temperature Range	SN54	Standard Commercial Processing

LOGIC AND LINEAR SNJ

Texas Instruments SNJ Logic and Linear Products are screened and processed in accordance with MIL-STD-883, Method 5004, Class B. Reference SNJ logic processing table. Electrical characteristics are as specified in the latest TI data sheets. All logic devices, except as noted, are tested for a 2% PDA after burn in. All Linear devices, except as noted, are tested for a 5% PDA after burn in.

DESC approved devices are tested and marked per appropriate DESC Military Drawing when Texas Instruments is an approved source.

Quality conformance inspection is performed per MIL-STD-883, Method 5005, and MIL-M-38510 paragraph 4.5, as noted in the lot conformance table.

All test programs have been audited to ensure compliance with published data sheets. Burn-in circuits and test programs are available for in-plant review.

Logic and Linear Screening and Lot Conformance—Class B

SCREEN	JM38510 Qualified		SNJ/B/DESC DWG/JEDEC Screening STD*	
	METHOD	RQMT	METHOD	RQMT
Internal Visual (Precap)	2010, Condition B Note 1	100%	2010, Condition B	100%
Stabilization Bake	Note 2		1008, Test Condition C min	100%
Temperature Cycling	1010, Condition C	100%	1010, Condition C	100%
Constant Acceleration	Note 2	100%	2001, Condition E (Min) in Y_1 Plane	100%
Seal Fine & Gross	1014	100%	1014	100%
Interim Electrical	JAN slash sheet, Note 3 Electrical Specifications	As applicable	TI Data Sheet Electrical specifications Note 3	Optional
Burn-In	1015 125°C Minimum PDA = JAN slash sheet	100%	1015, Notes 4, 5 125°C Minimum PDA LOG = 2%, LIN = 5%	100%
Final Electrical Tests a) Static Tests 1) 25°C (Subgroup 1, Table I, 5005) 2) Max and Min Rated Operating Temperature (Subgroups 2 & 3, Table I, 5005) b) Dynamic Tests, Note 8 25°C (Subgroup 4) Temp (Subgroup 5,6)	JAN slash sheet Electrical specifications	100%	TI Data Sheet Electrical specifications Notes 5, 6	100%

c) Switching Tests 25°C (Subroup 9, Table I, 5005)

d) Functional Tests
   1) 25°C (Subgroup 7, Table I, 5005)
   2) Max and Min Rated Operating Temperature (Subgroup 8, Table I, 5005)

Quality Conformance Inspection	5005 Class B	Sample Size	5005 Class B	Sample size
Group A Note 7				
a) Static				
1) 25°C (Subgroup 1)		116/0		116/0
2) Temp (Subgroups 2 & 3)		116/0		116/0, Note 5
b) Dynamic, Note 8				
1) 25°C (Subgroup 4)		116/0		116/0
2) Temp (Subgroups 5,6)		116/0		116/0
c) Switching, Note 8				
1) 25°C (Subgroup 9)		116/0		116/0, Notes 5, 11
2) Temp (Subgroups 10 & 11)		116/0		116/0
d) Functional				
1(25°C (Subgroup 7)		116/0		116/0
2) Temp (Subgroup 8)		116/0		116/0, Note 5
Group B	Table II B, 5005	Insp. Lot	Table II B, 5005	Insp. Lot
Group C	Table III, 5005	Wafer Fab/Qtr	Table III, 5005	52 Weeks Prod, Notes 5, 9, 10, 12
Group D	Table IV, 5005	35 Weeks Pkg. Prod.	Table IV, 5005	52 Weeks Pkg. Prod, Notes 5, 10
External Visual	2009	100%	2009	100%

*Per JEDEC Publication 101 Screening standard
See page 4 for the applicable notes for this table.

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NOTES: 1. Per MIL-STD-883, Method 5004, paragraph 3.3, alternate screening at manufacturer's option.
2. Per MIL-M-38510, Revision H, as of July 1, 1988, stabilization bake and constant acceleration requirements has been deleted.
3. Electrical stress test per MIL-STD-883, Method 5004, paragraph 3.3, if applicable.
4. Lower temperatures when required to limit T_j to 150 °C; however, parts will not be marked compliant.
5. For PALs only:
11. (a) PDA after burn-in = 5%
Electrical endpoints are Subgroups 1 and 7, Table I, and Method 5005.
Final electrical tests (Subgroups 10 and 11, Table I, and Method 5005) per TI data sheet electrical specifications.
6. Some data sheet parameters may be guaranteed via characterization data as identified in data book or military products testing exceptions section.
7. Per MIL-STD-883, Method 5005, paragraph 3.5.2.
8. When specified on slash/data sheets.
9. JM38510 generic data may be used.
10. Electrical endpoints are Subgroups 1, 2, 3, Table 1, and Method 5005.
11. (a) For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing Subgroup 9. Twenty-two devices shall be submitted to programming. If any devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 38 total devices with no more than one device failure allowable.
12. Effective Jan. 89, Group C QCI will be per Wafer Fab/Qtr/Microcircuit group.
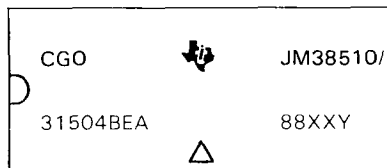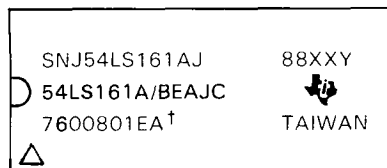
Symbolization

Example:	Order As:	Symbolization:

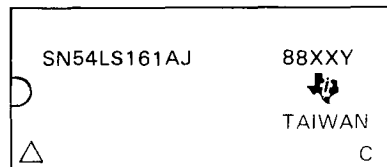**JANB**
54LS161A

JM38510/31504BEA

```
 CGO          🤠          JM38510/
)
  31504BEA                88XXY
        △
```

SNJ
54LS161A

SNJ54LS161AJ

```
  SNJ54LS161AJ        88XXY
) 54LS161A/BEAJC      🤠
  7600801EA†          TAIWAN
△
```

SN
54LS161A

SN54LS161AJ

```
  SN54LS161AJ         88XXY
)                     🤠
                      TAIWAN
△                           C
```

SNJ
Noncompliant Product

SNJ54S381J

```
  SNJ54S381J          88XXY
) 54S381/BRAJC        🤠
  NC                  TAIWAN
△
```
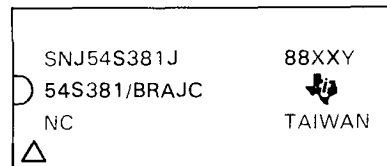
†Where TI is an approved source

Logic Cross-Reference Guide

Company	Class B Processing	Dual-in-line	Flatpack	Chip Carrier
TI	SNJ54XXX	J, JT	W	FK
Motorola	54XXX/BXXJC	C, E, R, J	A, D, F, K	2, 3, U
National	DM54XXX/883C MM54XXX/883C	J	W	
Fairchild	XXXXMQB	D	F	L1
Signetics	54XXX/BXX	F	W	G
RCA	CD54XXXX3	F	K	
MMI	SN54XXXX883B	J, JS	F	L
AMD	SN54XXXX/BXX	C, E, R, J	A, D, F, K	2, 3, U